Abstract of the Disclosure

Multiple passes of the loop of program verify and programming steps are performed for minimizing the effects of FG-FG coupling during programming a flash memory device. In one embodiment of the present invention, for programming a group of at least one flash memory cell of an array, a first pass of program verify and programming steps is performed until each flash memory cell of the group attains a threshold voltage that is at least X% of a program verify level but less than the program verify level. Then, a second pass of program verify and programming steps are performed until each flash memory cell of the group attains substantially the program verify level for the threshold voltage.